

CLAIMS

What is claimed is:

- 1 1. A semiconductor wafer, comprising:
 - 2 a planar semiconductor substrate;
 - 3 an elongated semiconductor element formed in the
 - 4 semiconductor substrate at a surface thereof, the semiconductor
 - 5 element being isolated from a surrounding conductive region of the
 - 6 semiconductor substrate by a buried oxide layer and side oxide
 - 7 layers; and
 - 8 a post disposed at one end of the semiconductor element, a
 - 9 side portion of the post being in contact with a conductive end
 - 10 portion of the semiconductor element, and a bottom portion of the
 - 11 post being in contact with the conductive region of the
 - 12 semiconductor substrate, the post being formed of a material
 - 13 effective (i) to provide for thermal and electrical coupling
 - 14 between the semiconductor element and the conductive region of the
 - 15 semiconductor substrate, and (ii) to provide for gettering
 - 16 impurities away from a surface portion of the semiconductor
 - 17 element during processing of the wafer.
- 1 2. A semiconductor wafer according to claim 1, wherein the post
- 2 material is polysilicon.
- 1 3. A semiconductor wafer according to claim 1, wherein the
- 2 semiconductor element comprises a sinker diffusion region at the
- 3 one end adjacent to the post, a drift region extending from the
- 4 sinker diffusion region toward the other end of the semiconductor
- 5 element, and a drain diffusion region at the other end of the
- 6 semiconductor element.

- 1 4. A semiconductor wafer according to claim 3, further comprising:
2 a layer of field oxide extending across the drift region on
3 the surface of the semiconductor element; and
4 a polysilicon gate on the field oxide above the drift region
5 adjacent to the sinker diffusion region.
- 1 5. A semiconductor wafer according to claim 3, further comprising:
2 a plurality of doped implants extending vertically in the
3 drift region adjacent to the sinker diffusion region to improve
4 the vertical spreading of current in the drift region.
- 1 6. A semiconductor wafer according to claim 1, wherein the
2 semiconductor element has a non-uniform end-to-end doping profile.
- 1 7. A semiconductor wafer according to claim 6, wherein the dopant
2 concentration varies linearly from one end of the semiconductor
3 element to the other end.
- 1 8. A semiconductor wafer according to claim 1, further comprising
2 a sidewall of insulating material adjacent to one side of the
3 semiconductor element, the sidewall having non-uniform width so as
4 to provide for relatively uniform electric field gradients in the
5 semiconductor element.
- 1 9. A semiconductor wafer according to claim 8, wherein the width
2 of the sidewall of insulating material varies linearly from one
3 end of the semiconductor element to the other end.
- 1 10. A method of processing a planar semiconductor substrate,
2 comprising:
3 forming spaced-apart trenches in the semiconductor substrate
4 at one surface thereof so as to define an elongated semiconductor
5 element;

6 passivating the upper portion of the semiconductor element
7 and performing a first oxidation process to create a buried oxide
8 layer beneath the passivated semiconductor element, the buried
9 oxide layer isolating the semiconductor element from a deeper
10 conductive region of the semiconductor substrate remaining after
11 the first oxidation process;

12 removing the passivation and performing a second oxidation
13 process to create an isolating side oxide layer on the sides of
14 the semiconductor element;

15 removing the side oxide layer and buried oxide layer at one
16 end of the semiconductor element so as to expose a conductive end
17 portion of the semiconductor element and an adjacent portion of
18 the conductive region of the semiconductor substrate; and

19 forming a post at the one end of the semiconductor element,
20 the post having a side portion in contact with the conductive end
21 portion of the semiconductor element and a bottom portion in
22 contact with the adjacent portion of the conductive region of the
23 semiconductor substrate, the post comprising a material effective
24 (i) to provide for thermal and electrical coupling between the
25 semiconductor element and the conductive region of the
26 semiconductor substrate, and (ii) to provide for gettering
27 impurities away from a surface portion of the semiconductor
28 element during subsequent processing of the semiconductor
29 substrate.

1 11. A method according to claim 10, wherein forming trenches
2 comprises:

3 passivating the one surface of the semiconductor substrate;
4 applying photoresist to the passivated surface in a pattern
5 defining the locations of the trenches;

6 etching the passivation at the locations of the trenches as
7 defined by the photoresist;

8 stripping the photoresist after etching the passivation; and

9 after stripping the photoresist, etching the trenches at the
10 locations defined by the non-passivated areas of the surface.

1 12. A method according to claim 10, further comprising:
2 filling the trenches with polysilicon after the isolating
3 side oxide layer has been created on the sides of the
4 semiconductor element; and
5 after filling the trenches with polysilicon, etch
6 planarizing the one surface of the semiconductor substrate.

1 13. A method according to claim 10, wherein the post material is
2 polysilicon.

1 14. A method according to claim 10, further comprising forming a
2 sinker diffusion region at the one end adjacent to the post, a
3 drift region extending from the sinker diffusion region toward the
4 other end of the semiconductor element, and a drain diffusion
5 region at the other end of the semiconductor element.

1 15. A method according to claim 14, further comprising:
2 forming a layer of field oxide extending across the drift
3 region on the surface of the semiconductor element; and
4 forming a polysilicon gate on the field oxide above the
5 sinker diffusion region.

1 16. A method according to claim 14, further comprising:
2 forming a plurality of doped implants extending vertically
3 in the drift region adjacent to the sinker diffusion region to
4 improve the vertical spreading of current in the drift region.

1 17. A method according to claim 10, further comprising doping the
2 semiconductor element in a non-uniform manner along its length.

1 18. A method according to claim 17, wherein the dopant
2 concentration varies linearly from one end of the semiconductor
3 element to the other end.

1 19. A method according to claim 10, further comprising forming a
2 sidewall of insulating material adjacent to one side of the
3 semiconductor element, the sidewall having non-uniform width so as
4 to provide for relatively uniform electric field gradients in the
5 semiconductor element.

1 20. A method according to claim 19, wherein the width of the
2 sidewall of insulating material varies linearly from one end of
3 the semiconductor element to the other end.